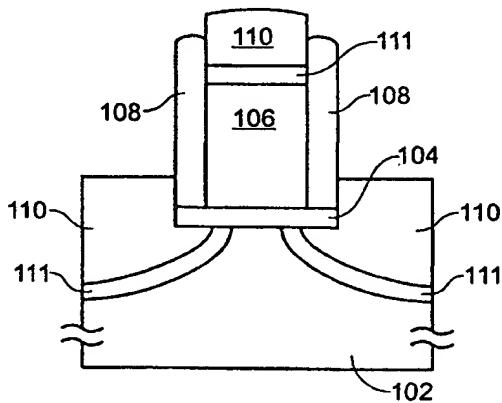


INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

| | | | |
|---|--|--|---|
| (51) International Patent Classification 6 : H01L 21/336 | | A1 | (11) International Publication Number: WO 00/30169 |
| | | | (43) International Publication Date: 25 May 2000 (25.05.00) |
| (21) International Application Number: PCT/US99/26224 | | (81) Designated States: AE, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CR, CU, CZ, DE, DK, DM, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, US, UZ, VN, YU, ZA, ZW, ARIPO patent (GH, GM, KE, LS, MW, SD, SL, SZ, TZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG). | |
| (22) International Filing Date: 5 November 1999 (05.11.99) | | | |
| (30) Priority Data: 09/191,076 12 November 1998 (12.11.98) US | | | |
| (71) Applicant (for all designated States except US): INTEL CORPORATION [US/US]; 2200 Mission College Boulevard, Santa Clara, CA 95052 (US). | | | |
| (72) Inventors; and | | Published | |
| (75) Inventors/Applicants (for US only): MURTHY, Anand, S. [IN/US]; Apartment 1304, 1845 N.W. 173rd Avenue, Beaverton, OR 97006 (US). CHAU, Robert, S. [US/US]; 13525 S.W. Harness Lane, Beaverton, OR 97008 (US). MORROW, Patrick [US/US]; 6150 N.W. Simnasho Drive, Portland, OR 97229 (US). JAN, Chia-Hong [-/US]; 395 N.W. 176th Avenue, Portland, OR 97229 (US). PACKAN, Paul [CA/US]; 15025 S.W. Gibralter Court, Beaverton, OR 97007 (US). | | With international search report. | |
| (74) Agents: MILLIKEN, Darren, J. et al.; Blakely, Sokoloff, Taylor & Zafman LLP, 7th floor, 12400 Wilshire Boulevard, Los Angeles, CA 90025 (US). | | | |

(54) Title: FIELD EFFECT TRANSISTOR STRUCTURE WITH ABRUPT SOURCE/DRAIN JUNCTIONS



(57) Abstract

Microelectronic structures embodying the present invention include a field effect transistor (FET) having highly conductive source/drain extensions. Formation of such highly conductive source/drain extensions includes forming a passivated recess which is back filled by epitaxial deposition of doped material to form the source/drain junctions. The recesses include a laterally extending region that underlies a portion of the gate structure. Such a lateral extension may underlie a sidewall spacer (108) adjacent to the vertical sidewalls of the gate electrode (106), or may extend further into the channel portion of a FET such that the lateral recess underlies the gate electrode portion of the gate structure. In one embodiment the recess is back filled by an in-situ epitaxial deposition of a bilayer of oppositely doped material. In this way, a very abrupt junction is achieved that provides a relatively low resistance source/drain extension and further provides good off-state subthreshold leakage characteristics. Alternative embodiments can be implemented with a back filled recess of a single conductivity type.